a first semiconductor chip having a main surface, a rear surface opposed to the main surface, and a plurality of electrode pads formed on the main surface, wherein the first semiconductor chip is mounted on the main surface of the wiring substrate with the rear surface of the first semiconductor chip facing to the main surface of the wiring substrate;

B' cont

a second semiconductor chip having a main surface, a rear surface opposed to the main surface, and a plurality of electrode pads formed on the main surface, wherein the second semiconductor chip is mounted on the main surface of the wiring substrate at the opposed side of the first row of electrode pads from the first semiconductor chip with the rear surface of the second semiconductor chip facing to the main surface of the wiring substrate;

a plurality of wires electrically connecting the electrode pads of the first semiconductor chip and the first row of electrode pads, respectively; and

a sealing material sealing the first and second semiconductor chips and the plurality of wires;

wherein an angle between the main surface of the wiring substrate and the wires at a portion of connecting the first row of electrode pads is larger than an angle between the main